AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method for parallel erase block tagging a plurality of memory devices each having a plurality of memory blocks, the method comprising:

transmitting an erase pulse to each of the plurality of memory blocks of each memory device, wherein only those blocks that are not erase block tagged receive the erase pulse;

determining a memory erase block status for the plurality of memory blocks; and

transmitting a parallel erase block tagging data burst to the plurality of memory devices, the data burst comprising erase block tag patterns for at least one of the memory devices.

2. (Original) The method of claim 1 wherein determining a memory block status comprises reading each memory cell in a memory block.

3. (Original) The method of claim 1 wherein writing the parallel erase block tagging data burst to the plurality of memory devices comprises writing a portion of the data burst to a first erase block latch in the at least one memory device.

4. (Original) The method of claim 3 wherein the portion of the data burst is converted to a logical address of the first erase block latch.

5. (Original) The method of claim 3 and further including continuing to transmit erase pulses to the plurality of memory blocks until all of the erase block latches indicate that the plurality of memory blocks of each of the plurality of memory devices are erased.

6. (Previously Presented) A method for parallel erase block tagging a plurality of memory devices each having a plurality of memory blocks including a plurality of memory cells, each memory block having an erase block latch, the method comprising:

transmitting an erase pulse to each of the plurality of memory blocks of each memory device, wherein only those blocks that are not erase block tagged receive the erase pulse;

reading the plurality of memory cells to determine the memory erase block status for each of the plurality of memory blocks; and

transmitting a parallel erase block tagging data burst to the plurality of memory devices, the data burst comprising a plurality of erase block tag patterns, each erase block tag pattern indicating which of the erase block latches to set in response to the memory erase block status.

7. (Original) The method of claim 6 and further including programming the plurality of memory blocks prior to transmitting the erase pulses.

8. (Original) The method of claim 6 wherein the plurality of memory devices are flash memory devices.

9. (Original) The method of claim 8 wherein the plurality of flash memory devices are NAND flash memory devices.

10. (Original) The method of claim 8 wherein the plurality of flash memory devices are NOR flash memory devices.

11. (Previously Presented) A method for parallel erase block tagging a plurality of memory devices in a testing apparatus, each memory device having a plurality of memory blocks organized into sectors and including a plurality of memory cells, each memory block having an erase block latch, the method comprising:

transmitting an erase pulse to each of the plurality of memory blocks of each memory device, wherein only those blocks that are not erase block tagged receive the erase pulse;

reading the plurality of memory cells to determine the memory erase block status for each of the plurality of memory blocks;

if at least one memory block is still programmed, generating an erase block tag pattern for each memory block still programmed;

generating a plurality of data bursts, each data burst comprised of erase block tag patterns for a predetermined sector address;

transmitting the plurality of data bursts to the plurality of memory devices, each erase block tag pattern indicating which of the erase block latches to set in response to the memory erase block status; and

setting the erase block latches in response to the erase block tag patterns.

12. (Original) The method of claim 11 and further including translating each erase block tag pattern received in a data burst to a logical address for a predetermined memory device.

13. (Previously Presented) An apparatus for parallel erase block tagging comprising:

a plurality of memory devices, each memory device comprising a plurality of memory blocks, each memory block having an erase block tag latch that prevents erase pulses transmitted to a particular memory block from being received by the memory block;

a plurality of data input/output lines coupled to the plurality of memory devices; and

a processor coupled to the plurality of data input/output lines for controlling testing operations of the plurality of memory devices, the processor capable of generating data bursts comprising a plurality of erase block tag patterns that are transmitted to each of the plurality of memory devices in parallel.

14. (Original) The apparatus of claim 13 and further including a plurality of bit line drivers, each bit line driver coupled between a data input/output line and a memory device.

15. (Original) The apparatus of claim 14 and further including a plurality of data latches, each data latch coupled between a data input/output and a bit line driver.

16. (Original) The apparatus of claim 13 wherein the plurality of memory devices are capable of decoding a received erase block tag pattern from a data burst into a logical address corresponding to an erase block tag latch.

17. (Original) The apparatus of claim 13 and further including a plurality of bit line drivers coupled to global bit lines of the memory device such that the plurality of erase block tag patterns are transmitted to the plurality of erase block latches over the global bit lines.

18. (Original) The apparatus of claim 13 wherein each of the plurality of memory devices is capable of setting, substantially simultaneously, a first erase block tag latch in response to a received erase block tag pattern.

19. (Previously Presented) An electronic system for parallel erase block tagging of memory devices, the system comprising:

a plurality of memory devices, each memory device comprising a plurality of memory blocks, each memory block having an associated erase block tag latch that prevents erase pulses transmitted to a particular memory block from being received by the memory block;

a plurality of data input/output lines coupled to the plurality of memory devices; and

a processor coupled to the plurality of data input/output lines for controlling testing operations of the plurality of memory devices, the processor capable of transmitting an erase pulse to the plurality of memory blocks that are not erase block tagged, determining a memory erase block status for the plurality of memory blocks, and transmitting a parallel erase block tagging data burst substantially simultaneously to the plurality of memory devices, the data burst comprising erase block tag patterns for setting an associated erase block tag latch in the plurality of the memory devices.

20. (Original) The system of claim 19 wherein an erase block tag latch is set when it has a logic high state.

21. (Previously Presented) A method for parallel erase block tagging a plurality of memory devices each having a plurality of memory blocks including a plurality of memory cells, each memory block having an erase block latch, the method comprising:

transmitting an erase pulse to each of the plurality of memory blocks of each memory device, wherein only those blocks that are not erase block tagged receive the erase pulse;

reading the plurality of memory cells to determine the memory erase block status for each of the plurality of memory blocks; and

transmitting a parallel erase block tagging data burst to the plurality of memory devices, the data burst comprising a plurality of erase block tag patterns each having an equivalent logical state such that when the plurality of memory devices receive the erase block tag patterns, the erase block latches are set to a predetermined state.

22. (Original) The method of claim 21 wherein the predetermined state is an erased state.

23. (Original) The method of claim 21 wherein the predetermined state is an unerased state.

24. (Original) The method of claim 21 wherein the equivalent logical state is a logic low.